Avoiding Audible Noise at Light Loads When Using Leading Edge Triggered PFC Converters

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This application note applies to the TI average current mode, leading edge modulation PFC controllers. See Applicable Device Table for part numbers.

When using a leading edge triggered PFC the designer may find that the converter under extremely light load conditions will encounter an audible low noise.

The unit under these conditions can go into the over voltage protection (OVP) state because of the extremely light load. When this happens, the output of the current error amplifier can fall to ground because of the input offset voltage variations and the residual current from MOUT.

When the unit comes out of the OVP state, the pulse width of the converter is going to start at a maximum. Because of the integrating nature of the error amplifier, these pulses will continue for a few milliseconds. This can cause the windings of the PFC inductor to physically oscillate resulting in a periodic burst of audible noise.

A single resistor from V_{REF} to the positive input of the current error amplifier added to the circuit is sufficient to remove this problem.

The input offset voltage of the error amplifier and the multiplier zero current (I_{MOUT}, zero current) are given in the data sheet. Divide the offset voltage by the value of the resistor connecting the positive input of the current error amplifier to ground and add to this the multiplier zero current. This gives the current needed through the resistor to bias the positive input high under OVP conditions. Now divide the VREF voltage by this current to get the resistor needed to connect from VREF to the positive input of the current error amplifier.

The new resistor will bias the positive input high enough to keep the current error amplifier output high during OVP and because of the integrating nature of the current error amplifier, when OVP is released the unit will gradually increase the pulse width of the pulses as the current error amplifier output falls.

1 Schematic

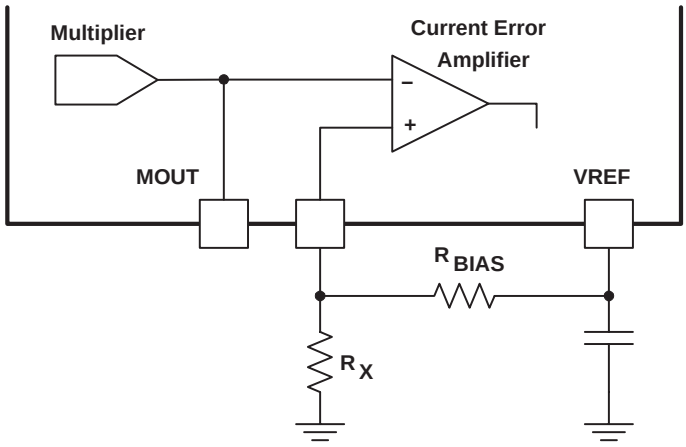

Figure 1.

Where R_X is the existing resistor from the positive input of the current error amplifier to ground,

$$I_{BIAS} = \frac{V_{OFFSET}}{R_X}$$

$$R_{BIAS} = \frac{V_{REF}}{\left(I_{BIAS} + I_{MOUT},\ zero\ current\right)}$$

Select the nearest standard value lower than this for R_{BIAS}.

Table 1. Applicable Devices

BiCMOS Power Factor Preregulators		BiCMOS PFC/PWM Combination Controllers	
UCC2817	UCC2817A	UCC28500	UCC28510
UCC2818	UCC2818A	UCC28501	UCC28511
UCC2819	UCC2819A	UCC28502	UCC28512
UCC3817	UCC3817A	UCC28503	UCC28513
UCC3818	UCC3818A	UCC38500	UCC28514
UCC3819	UCC3819A	UCC38501	UCC28515
		UCC38502	UCC28516
		UCC38503	UCC28517

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