Application Note AN42009 (ML AN33)

ML4824 Combo Controller Applications

General Description

This Application Note shows the step-by-step process to design a high performance supply. The equations shown in this document can also be used for different output voltages and total power.

The complete power supply circuit shown in Figure 6 demonstrates the ML4824's ability to manage high output power while easily complying with international requirements regarding AC line quality. The PFC section provides $380V_{DC}$ to a dual transistor current-mode forward converter. The output of the converter delivers +12V at up to 16 amps. The circuit operates from 80 to $264V_{AC}$ with both power sections switching at 100kHz.

The PFC Stage

Powering the ML4824

The ML4824 is initialized once C_{30} is charged to 13V through R_{27} and R_{30} . PFC switching action now boosts the voltage on C_5 to 380V via T_1's primary inductance. T_1 then supplies a well regulated 13V for the ML4824 from its secondary winding and full wave rectifier consisting of D_3 , D_4 , C_{10} and C_{11} . T_1's primary to secondary turns ratio (N_{PRI} / N_{SEC}) is 25.5:1. For proper circuit operation, high frequency bypassing with low ESR ceramic or film capacitors on V_{CC} and V_{REF} is provided. Orderly PFC operation upon start-up is guaranteed when D_2 quick charges the boost capacitor to the peak AC line voltage before the boost switch

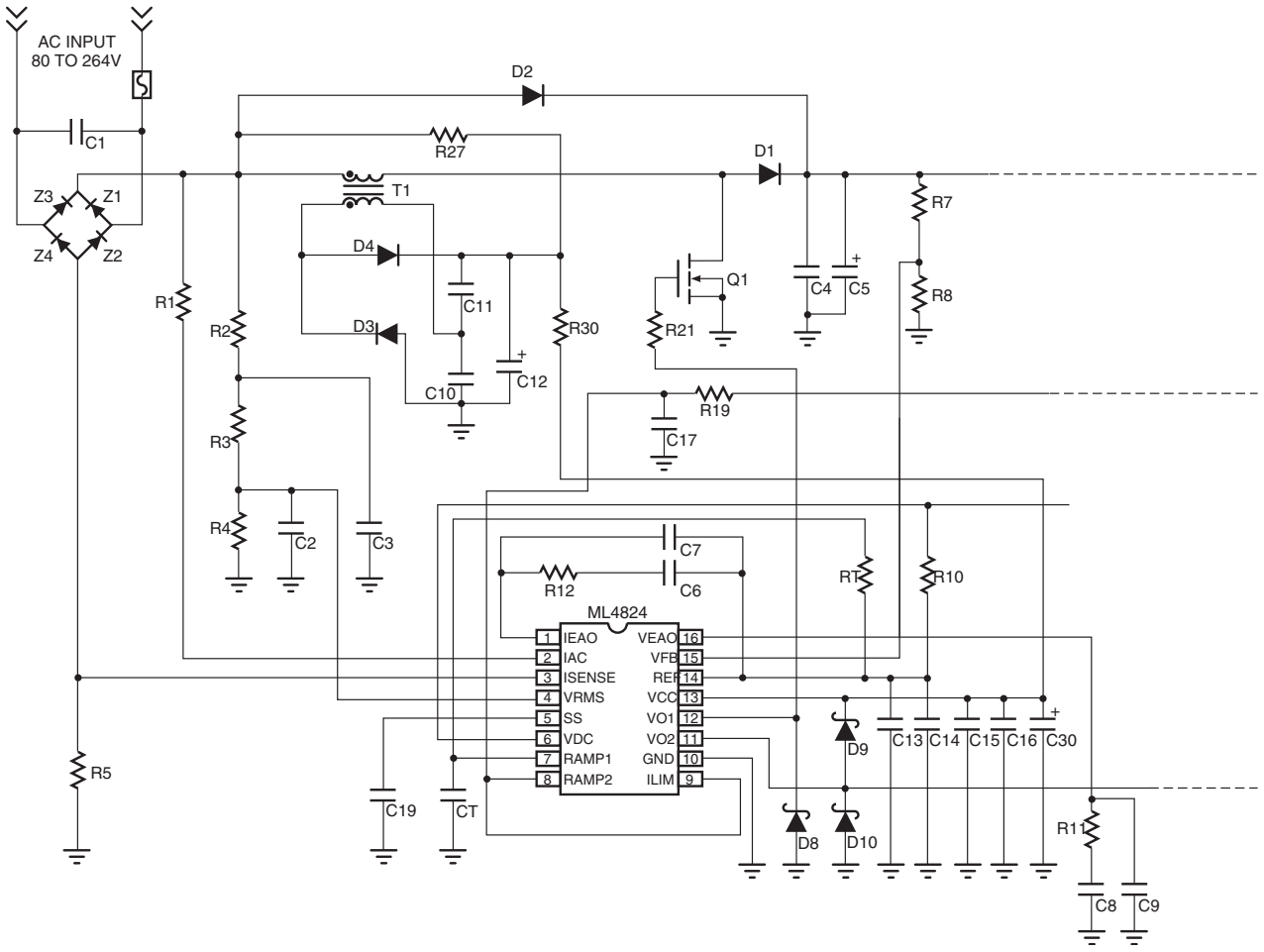

Figure 1. The PFC Stage

Q_1 is turned on. This ensures the boost inductor current is zero before PFC action begins. The value of the regulated voltage on C_5 must always be greater than the peak value of the maximum line voltage delivered to the supply.

$$V_{C5} > \sqrt{2}V_{RMS(MAX)}$$
$$V_{C5} > (1.414)(264)$$
$$V_{C5} > 373\,V \text{ use } 380\,V \quad (1)$$

Because the ML4824 uses transconductance amplifiers the loop compensation networks are returned to ground (see the ML4824 data sheet for the error amplifier characteristics/ advantages). This eliminates the interaction of the resistive divider network with the loop compensation capacitors permitting a wide choice of divider values chosen only to minimize amplifier offset voltages due to input bias currents. For reliable operation R_7 must have a voltage rating of at least 400 volts.

Calculate the resistor divider ratio R_7/R_8.

$$\frac{R_7}{R_8} = \frac{V_{C5}}{2.50} - 1$$
$$\frac{R_7}{R_8} = \frac{380}{2.5} - 1$$
$$\frac{R_7}{R_8} = 151 \quad (2)$$

Selecting the Power Components

The ML4824 PFC section operates with continuous inductor current to minimize peak currents and maximize the available power. The inductance value required for continuous current operation in the typical application is found in equation 3.

$$T_{1(PRI)} = \frac{0.445\,V_{RMS(MAX)}{}^2}{(f_{PFC})(P_{OUT})}$$
$$T_{1(PRI)} = \frac{(0.445)(264)^2}{(1\times 10^5)(200)}$$
$$T_{1(PRI)} = 1.55\,mH \text{ use } 1.5\,mH \quad (3)$$

The boost diode D_1 and switch Q_1 are chosen with a reverse voltage rating of 500V to safely withstand the 380V boost potential. The average and peak currents respectively through these components are:

$$I_{AVG} = \frac{\pi P_{OUT}}{2\sqrt{2}\,V_{RMS(MIN)}}$$
$$I_{AVG} = \frac{(3.1416)(200)}{(2)(1.414)(80)}$$
$$I_{AVG} = 2.78A \quad (4)$$

$$I_{PEAK} = \frac{\pi I_{AVG}}{2}$$
$$I_{PEAK} = \frac{(3.1416)(2.78)}{2}$$
$$I_{PEAK} = 4.37A \quad (5)$$

The boost capacitor value is chosen to permit a given output voltage hold-up time in the event the line voltage is suddenly removed.

$$C_5 \geq \frac{2(P_{OUT})(t_{HLD})}{V_{C5(NOM)}{}^2 - V_{C5(MIN)}{}^2} \quad (6)$$

Where:

t_{HLD} = hold-up time (sec)

$V_{C5(MIN)}$ = minimum voltage on C_5 at which the PWM stage can still deliver full output power

A key advantage of using leading/trailing edge modulation is that a large portion of the inductor current is "dumped" directly into the load (PWM stage transformer) and not the boost capacitor. This relaxes the ESR requirement of the boost capacitor. For reference, equation 7 should be used as a starting point when choosing C_5's maximum ripple current rating (at 120Hz).

$$I_{RMS(C5)} = \frac{I_{OUT\,(C5)}}{\sqrt{2}} \quad (7)$$

$$\left(I_{PEAK} = \sqrt{2}\,I_{RMS(C5)}\right) \quad (7a)$$

Selecting the Power Setting Components

The maximum average power delivered by the PFC stage is easily set using the following procedure:

1. Find the resistive divider ratio that results in the voltage at the V_{RMS} pin being equal to 1.20V at the lowest line voltage. The voltage at this pin must be well filtered and yet able to respond well to transient line voltage changes.

$$\frac{R_4}{R_{TOT}} = \frac{1.20\pi}{2\sqrt{2}\,V_{RMS(MIN)}} \quad (8)$$

The resistor and capacitor values in the typical example were found empirically to offer the lowest ripple voltage and still respond well to line voltage changes. Should a ratio be required which is greatly different from that found in equation 8, adjust the filter capacitor values according to equations 9 and 10.

$$C_3 = \frac{R_{TOT}}{2\pi f_1 R_2 (R_3 + R_4)} \quad (9)$$

$$C_2 = \frac{\left(1 + \frac{R_4 R_{TOT}}{R_2(R_3 + R_4)}\right)}{2\pi f_2 R_4} \quad (10)$$

Where:

f_1 = 15Hz, f_2 = 23Hz

$R_{TOT} = R_2 + R_3 + R_4$

2. Find the constant of proportionality k_m of the multiplier gain k in equation 11a. To obtain "brown-out" action below the lowest input voltage the maximum gain of the multiplier must be used when finding k_M. The maximum gain (0.328) occurs when the V_{RMS} input of the multiplier is 1.20V. Equation 11(ref) is the general expression for the multiplier gain versus the line voltage.

$$k = \frac{k_M}{V_{RMS}^2}(\text{ref}) \quad (11)$$

$$k_M = k\, V_{RMS(MIN)}^2$$
$$k_M = (0.328)(80)^2 \quad (11a)$$
$$k_M = 2099$$

3. Now select the value of R_1 which permits the greatest multiplier output current without saturating the output. The maximum output current of the multiplier is 200µA.

$$R_1 \geq \frac{k\sqrt{2}V_{RMS(MIN)}(V_{EAO} - 1.5)}{200 \times 10^{-6}}$$

$$R_1 \geq \frac{(0.328)\sqrt{2}(80)(6.8 - 1.5)}{200 \times 10^{-6}} \quad (12)$$

$$R_1 \geq 983\text{k}\Omega \text{ use } 1\text{M}\Omega$$

4. Selecting the value of the current sense resistor completes the calculations for the power setting components.

$$R_5 \leq \frac{R_{MULO}(V_{EAO} - 1.5)k_M}{(R_1)(P_{OUT})}$$

$$R_5 \leq \frac{(3500)(6.8 - 1.5)(2099)}{(1 \times 10^6)(200)} \quad (13)$$

$$R_5 \leq 0.195\Omega \text{ use } 0.15\Omega$$

Where:

R_{MULO} = multiplier output termination resistance (3.5k)

Voltage Loop Compensation

Maximum transient response of the PFC section, without instability, is obtained when the open loop crossover frequency is one-half the line frequency. For this application the compensation components (pole/zero pair) are chosen so that the closed loop response decreases at 20dB/decade, crossing unity gain at 30Hz, then immediately decreasing at 40dB/decade. The error amplifier pole is placed at 30Hz and an effective zero at one-tenth this frequency or 3Hz. First find the crossover frequency (G_{PS} = 1) of the power stage. For reference, equation 15 finds the power stage pole, equation 16 the power stage DC gain.

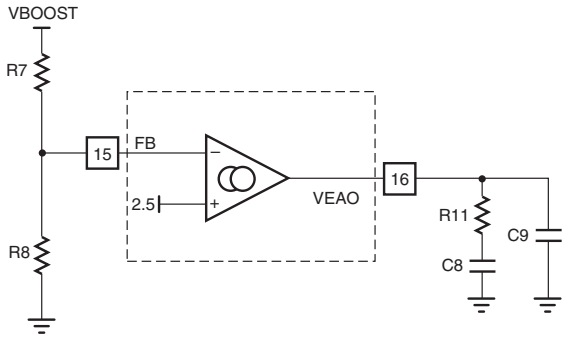

Figure 2. Voltage Amp Compensation

$$f_C = \frac{P_{IN(AVG)}}{2\pi V_{C5} V_{EAO(MAX)} C_5}$$

$$f_C = \frac{200}{(2)(3.1416)(380)(5.3)(270 \times 10^{-6})} \quad (14)$$

$$f_C = 58.5\text{Hz}$$

$$f_P = \frac{1}{\pi R_L C_5}$$

$$f_P = \frac{1}{(3.1416)(722)(270 \times 10^{-6})} \quad (15)$$

$$f_P = 1.63\text{Hz}$$

Where:

$$R_L = \frac{V_{C5}{}^2}{P_{OUT}}$$

$$G_{PS(DC)} = \frac{\sqrt{2}\, f_C}{f_P}$$

$$G_{PS(DC)} = \frac{(1.414)(58.5)}{(1.63)} \quad (16)$$

$$G_{PS(DC)} = 50.1 (34.1dB)$$

Now the gain of the power stage at 30Hz is calculated.

$$G_{PS(30Hz)} = \frac{f_C}{30}$$

$$G_{PS(30Hz)} = \frac{58.5}{30} \quad (17)$$

$$G_{PS(30Hz)} = 1.95 (5.8dB)$$

The power stage gain will be attenuated by the resistive divider R_7/R_8 according to equation 18.

$$G_{RDIV} = \frac{R_8}{R_7 + R_8}$$

$$G_{RDIV} = \frac{(2.37)}{(357 + 2.37)} \quad (18)$$

$$G_{RDIV} = 6.59 \times 10^{-3} \ (-43.6dB)$$

The amount of error amplifier gain required to bring the open loop gain to unity at 30Hz is the negative of the sum of the power stage plus divider stage gain (attenuation):

$$G_{EA} = -(G_{PS(30)} + G_{RDIV})$$

$$G_{EA} = -(5.8 + (-43.6)) \quad (19)$$

$$G_{EA} = 37.8dB \ (77.6V / V)$$

The value of R_{11}, which sets the high frequency gain of the error amplifier, can now be determined.

$$R_{11} = \frac{G_{EA}}{g_M}$$

$$R_{11} = \frac{77.6}{85 \times 10^{-6}} \quad (20)$$

$$R_{11} = 915K \text{ use } 910K$$

Calculate C_8 which together with R_{11} sets the zero frequency at 3Hz.

$$C_8 = \frac{1}{2\pi R_{11} f_Z}$$

$$C_8 = \frac{1}{(2)(3.1416)(910K)(3)} \quad (21)$$

$$C_8 = 58nF \text{ (use } 56nF)$$

Since the pole frequency is ten times the zero frequency the pole capacitor C_9 will be one-tenth the value of C_8.

$$C_9 = \frac{C_8}{10}$$

$$C_9 = \frac{56 \times 10^{-9}}{10} \quad (22)$$

$$C_9 = 5.6nF$$

Current Loop Compensation

The current loop is compensated exactly like the voltage loop with the exception of the choice of the open loop crossover frequency. To prevent interaction with the voltage loop, the current loop bandwidth should be greater than ten times the voltage loop crossover frequency but no more than one-sixth the switching frequency or 16.7kHz. The power stage crossover frequency is found in equation 23, the pole frequency in 24 and for reference the power stage DC gain is found in equation 25.

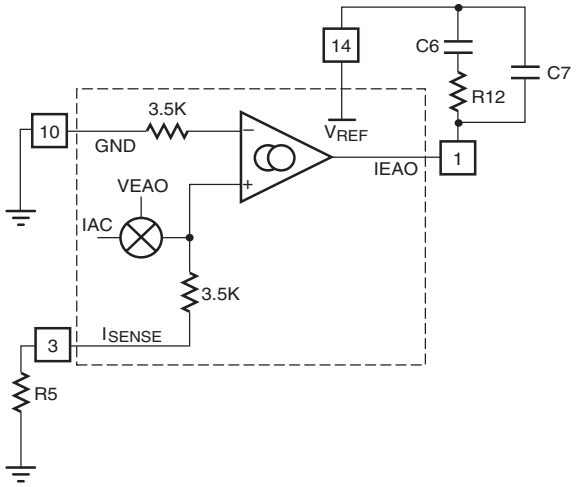

Figure 3. Current Amp Compensation

$$f_C = \frac{R_5 V_{C5}}{2\pi T_{1(PRI)} V_{RAMP(P-P)}}$$

$$f_C = \frac{(0.15)(380)}{(2)(3.1416)(1.5\times10^{-3})(2.5)} \quad (23)$$

$$f_C = 2.42\text{kHz}$$

$$f_P = \frac{1}{\pi R_L C_5}$$

$$f_P = \frac{1}{(3.1416)(722)(270\times10^{-6})} \quad (24)$$

$$f_P = 1.63\text{Hz same as equation 15}$$

$$G_{PS(DC)} = \frac{\sqrt{2} f_C}{f_P}$$

$$G_{PS(DC)} = \frac{(1.414)(2.42\times10^3)}{(1.63)} \quad (25)$$

$$G_{PS(DC)} = 2099\,(66.4\text{dB})$$

Find the gain of the power stage at 16.7kHz.

$$G_{PS(16.7\text{kHz})} = \frac{f_C}{16.7\times10^3}$$

$$G_{PS(16.7\text{kHz})} = \frac{2.42\times10^3}{16.7\times10^3} \quad (26)$$

$$G_{PS(16.7\text{kHz})} = 1.45\times10^{-1}(-16.8\text{dB})$$

The current loop contains no attenuating resistors so proceed to find the error amplifier gain in equation 27.

$$G_{EA} = -(-G_{PS(16.7\text{kHz})})$$

$$G_{EA} = -(-16.8) \quad (27)$$

$$G_{EA} = 16.8\text{dB (6.9V / V)}$$

Now determine the value of the current error amplifier setting resistor R_{12}.

$$R_{12} = \frac{G_{EA}}{g_m}$$

$$R_{12} = \frac{6.9}{195\times10^{-6}} \quad (28)$$

$$R_{12} = 35.4\text{k use 36k}$$

Calculate the value of C_6 to form the zero at 1.6kHz.

$$C_6 = \frac{1}{2\pi R_{12} f_Z}$$

$$C_6 = \frac{1}{(2)(3.1416)(36\times10^3)(1.67\times10^3)} \quad (29)$$

$$C_6 = 2.6\text{nF (use 2.7nF)}$$

The pole capacitor C_7 is one-tenth the value of C_6.

$$C_7 = \frac{C_6}{10}$$

$$C_7 = \frac{2.7\times10^{-9}}{10} \quad (30)$$

$$C_7 = 270\text{pF}$$

The PWM Stage

Soft-Starting the PWM Stage

The ML4824 features a dedicated soft-start pin for controlling the rate of rise of the output voltage and preventing overshoot during power on. The controller will not initiate soft-start action until the PFC voltage reaches its nominal value thereby preventing stalling of the output voltage due to excessive PFC currents. Furthermore, PWM action will be terminated in the event that the ML4824 loses power or if the PFC boost voltage should fall below $228V_{DC}$. The soft-start capacitor value (C_{19}) for 25ms of delay is found in equation 31.

$$C_{19} = (t_{SS})\left(\frac{50\times10^{-6}}{1.25}\right)$$

$$C_{19} = (0.025)\left(\frac{50\times10^{-6}}{1.25}\right) \quad (31)$$

$$C_{19} = 1\mu\text{F}$$

Setting the Oscillator Frequency

There are two versions of the ML4824. The ML4824-1 where the PFC and PWM run at the same frequency and ML4824-2 where the PWM stage is 2X PFC frequency.

ML4824-1

In general it is best to choose a small valued capacitor C_1 to maximize the oscillator duty cycle (minimize the C_1 discharge time). Too small a value capacitor can increase the oscillator's sensitivity to phase modulation caused by stray field voltage induction into this node. For the practical example a 470pF capacitor was first chosen for C_1. Equation 32 is accurate with values of R_1 greater than 10k.

$$R_T \cong \frac{1}{0.51 f_{SW} C_T}$$

$$R_T \cong \frac{1}{0.51(1\times10^5)(470\times10^{-12})} \quad (32)$$

$$R_T \cong 41.2\text{k}$$

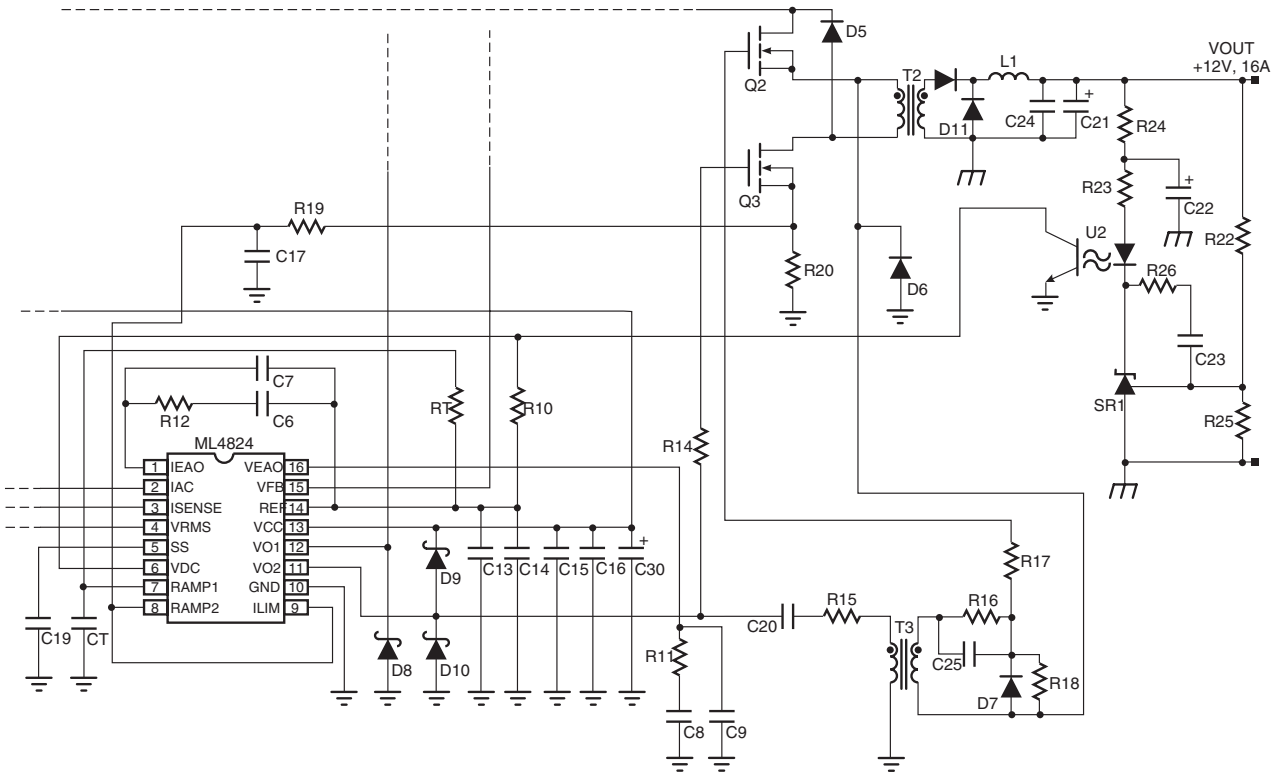

Figure 4. The PWM Stage

ML4824-2

The ML4824-2 allows the user to operate the PWM stage at twice the PFC frequency, thereby reducing the physical size of the PWM stage magnetics and filter components. The PFC frequency is the same as the external oscillator frequency. The PWM frequency is formed by comparing the oscillator ramp voltage to internal voltage references which ideally make the duty cycle of the 2 waveforms generated during each oscillator cycle identical. The PWM section duty cycle must be balanced to minimize phase jitter. This is accomplished by making the oscillator dead-time (C_1 discharge time) equal to 2.5% of the total period. First choose the C_1 value from equation 33.

$$C_T \cong \frac{0.025}{490\ fsw} \qquad (33)$$

Now R_1 is found from equation (34) which is identical to equation 32.

$$R_T \cong \frac{1}{0.51\,fsw\,C_T} \qquad (34)$$

As a final test, an in-circuit check of 2 adjacent PWM cycles should be examined for duty cycle balance. For more detail involving duty cycle balancing please refer to Application Note 34.

Current Limit

The PWM power stage operates in current mode using R_{20} to generate the voltage ramp for duty cycle control. The ML4824 limits the maximum primary current via an internal 1_V comparator which when exceeded terminates the drive to the external power MOSFETs. Maximum primary current is:

$$I_{PRI\,(MAX)} = \frac{1}{R_{20}}$$

$$I_{PRI\,(MAX)} = \frac{1}{0.5} \qquad (35)$$

$$I_{PRI\,(MAX)} = 2Amps$$

Voltage Mode (Feed-Forward)

Should voltage mode control be used it is necessary to know C_5's peak voltage in order to choose the correct ramp generating components. Equation 36 finds the worse case peak to peak ripple voltage across C_5. To find the peak voltage divide the ripple voltage by two and add it to the regulated boost voltage. Remember that since the ML4824 employs leading/trailing modulation the actual peak to peak ripple voltage will generally be much less than the calculated value.

$$V_{R(C5)} = I_{OUT\,(C5)} \sqrt{\left(\frac{1}{4\pi f_L C_5}\right)^2 + ESR(C_5)^2} \qquad (36)$$

Where:

f_L = line frequency

Solve equation 37 for the ramp resistor value. The ramp capacitor value should be in the range of 470pF – 10000pF. Choose a resistor with an adequate voltage rating to withstand the boost voltage.

$$R_{RAMP} = \frac{\sigma_{(MAX)}}{C_{RAMP} f_{SW} 1n\left(1 - \frac{V_{REF}}{V_{C5} + 0.5V_R}\right)} \quad (37)$$

Where:

$\sigma_{(MAX)}$ = maximum PWM duty cycle (0.45 for the ML4824-1)

V_R = peak to peak boost capacitor ripple voltage (equation 36)

The Power Transformer Turns Ratio

The minimum output voltage at the secondary of T_2 is found in equation 38.

$$V_{SEC(MIN)} = \frac{V_{OUT}}{\sigma_{(MAX)}} + V_F$$

$$V_{SEC(MIN)} = \frac{12}{0.45} + 1.0 \quad (38)$$

$$V_{SEC(MIN)} = 27.7 \text{ Volts}$$

The secondary voltage was chosen to be 30 volts to increase the output voltage hold up time. The transformer turns ratio is easily found from equation 39.

$$\frac{N_{PRI}}{N_{SEC}} = \frac{V_{C5}}{V_{SEC(MIN)}}$$

$$\frac{N_{PRI}}{N_{SEC}} = \frac{380}{30} \quad (39)$$

$$\frac{N_{PRI}}{N_{SEC}} = 38:3$$

The maximum secondary current with the output shorted is limited by equation 40.

$$I_{SEC(MAX)} = \frac{I_{PRI(MAX)} N_{PRI}}{N_{SEC}}$$

$$I_{SEC(MAX)} = \frac{(2)(38)}{3} \quad (40)$$

$$I_{SEC(MAX)} = 25.3 \text{ Amps}$$

The output inductor and rectifier were chosen with maximum current ratings larger than the maximum secondary current.

Output Filter Component Filter Selection

L_1's value was chosen to efficiently minimize output ripple current thereby easing the ESR requirement of the filter capacitor. C_{21}'s ESR value is the dominant contributor to the output ripple. The maximum ESR value required is found in equation 41.

$$ESR_{(C21)} \leq \frac{V_R L_1 f_{SW}}{V_{SEC} \sigma_{(MAX)}} \quad (41)$$

Where:

V_R = peak to peak output ripple voltage

Output Voltage Compensation

A LM431 shunt regulator SR_1 and opto-isolator U_2 perform output voltage setting and regulation. The opto crosses the primary to secondary safety boundary varying the voltage on the VDC pin to keep the output voltage constant against line and load changes. Using current mode control simplifies loop compensation leaving only a single pole and zero in the output stage. The pole is created from the output capacitor and equivalent load resistance. The zero is formed from the filter capacitor and its ESR. In this example, the action of the zero occurs well after the closed loop response has crossed unity, so it was not compensated with a pole. The output pole is canceled increasing the overall bandwidth by the addition of R_{26} and C_{23} which form a zero with LM431. For more information on using the LM431, including gain/phase versus frequency characteristics, please refer to the Texas Instruments Linear Data Handbook.

3.3V Output Design Changes

The latest microprocessors and support circuitry require a 3.3V supply for proper operation. The ML4824 is ideal for these applications including the energy efficient, ecologically friendly "Green PC's". If the total output power required varies greatly from 200 watts it will be necessary to re-select certain components beginning with the PFC stage. T_2's turn ratio must be adjusted according to equation 39 and another low current secondary winding added using the same turns ratio as originally found for the +12 volts. This second winding is necessary to power the LM431/opto circuit as the 3.3V output is not adequate to fully bias the feedback circuitry. C_{21} may be increased to reduce the output ripple voltage. The figure below displays a 3.3V output stage capable of supplying 16 amps.

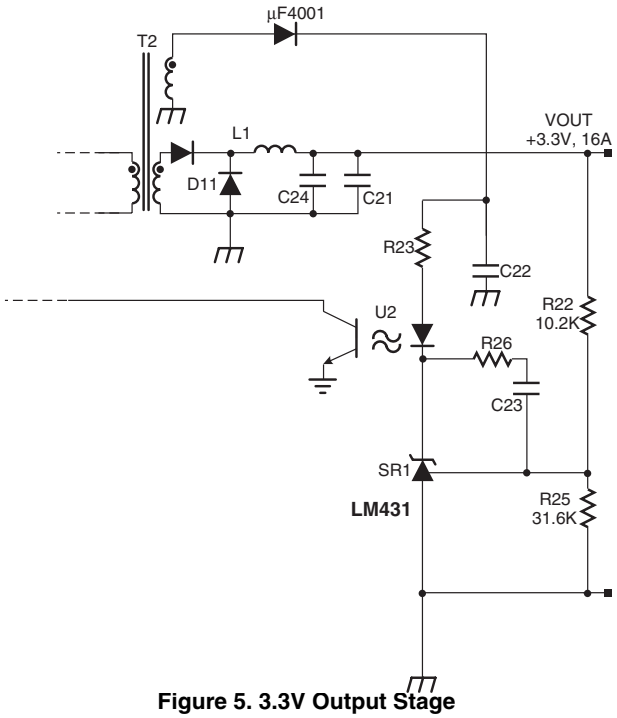

Figure 5. 3.3V Output Stage

Note: For more information see Application Note 34.

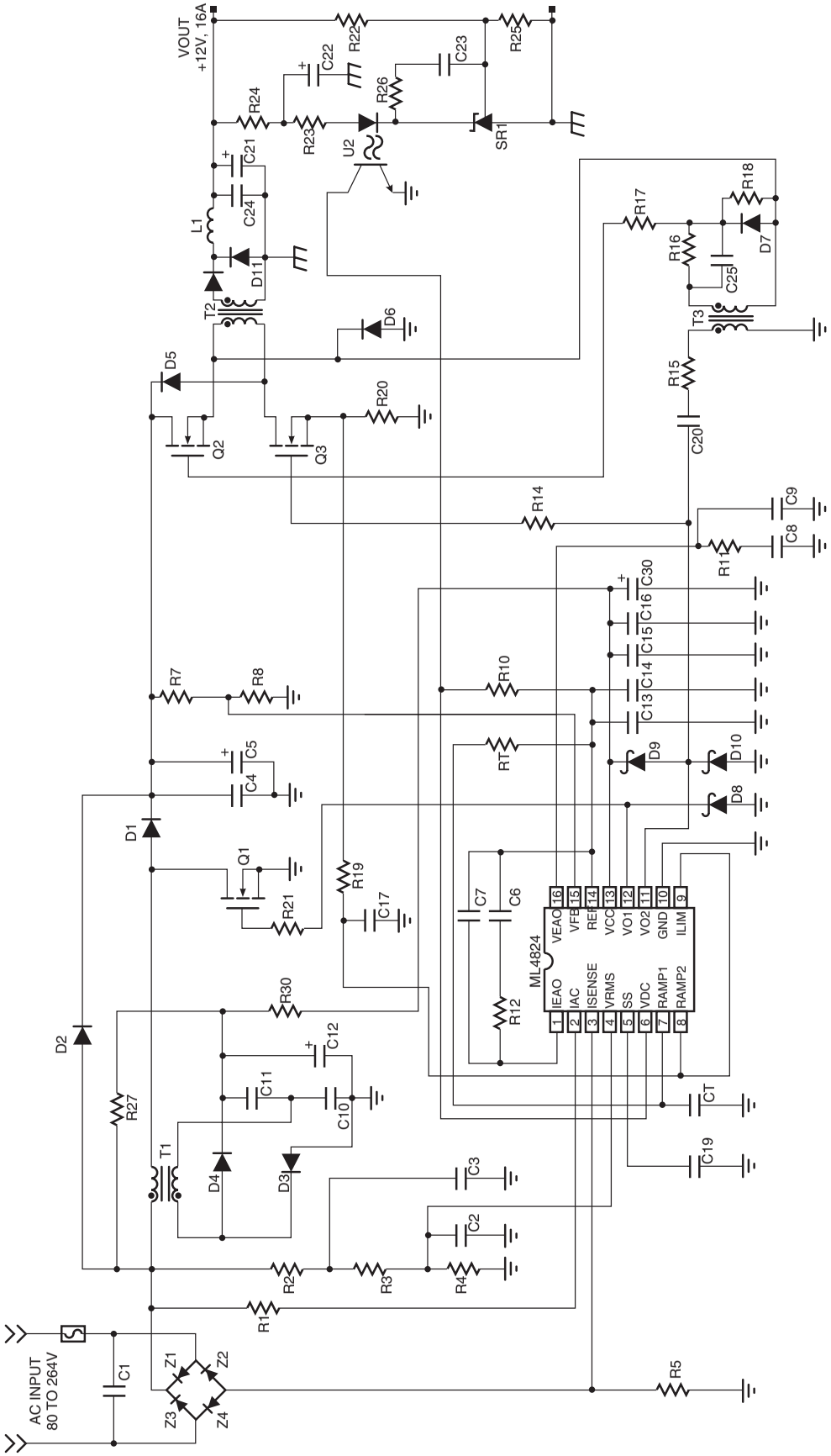

Figure 6. Complete 200W Circuit